AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-3 (Cancelled)

4. (Currently Amended) A semiconductor integrated circuit device ~~according to claim 1, wherein~~, comprising:

a latch provided on an output of a memory circuit;

wherein said latch includes a signal selector for switching between feedback signal of normal operation and test signal of test operation in compliance with an operation mode signal to send out to a feedback loop;

~~said latch is provided at the output of said memory;~~

wherein said latch has a first switch for sending ~~the~~ a read-out signal from a memory cell in said memory circuit to an input terminal of a first inverter under ~~the~~ control of a switch control signal, a second inverter for receiving ~~the~~ an output signal of said first inverter on ~~the~~ an input terminal, and a second switch for sending ~~the~~ an output signal of said second inverter to the input terminal of said first inverter under ~~the~~ control of said switch control signal, and said latch outputs a latch output signal from

~~the~~ an output terminal of said second inverter;

said signal selector has a third switch for sending ~~the~~ an input signal fed to said memory circuit to the input terminal of said first inverter as the test signal under ~~the switching~~ control of said switch control signal, and a signal generator for generating said switch control signal; and

said signal generator turns off said third switch in the normal operation by said operation mode signal to perform a complementary switching control of said first and second switches by using clock pulses as said switch control signal, and turns off said first and second switches and turns on said third switch in the test operation by said operation mode signal.

5. (Currently Amended) A semiconductor integrated circuit device ~~according to claim 1, wherein~~, comprising:

a latch provided on an input of a logic circuit;

wherein said latch includes a signal selector for switching between feedback signal of normal operation and test signal of test operation in compliance with an operation mode signal to send out to a feedback loop;

~~said latch is provided at the input of said logic;~~

said latch includes a first latch for receiving ~~the~~ an

input signal in the normal operation and a second latch for generating the signal input to said logic circuit upon reception of ~~the~~ an output from said first latch; and

said signal selector is provided in ~~the~~ a feedback loop of said first latch.

6. (Currently Amended) A semiconductor integrated circuit device according to claim 5, wherein:

said first latch has a first switch for sending said input signal to ~~the~~ an input terminal of a first inverter under ~~the switching~~ control of a switch control signal, a first clocked inverter for receiving ~~the~~ an output signal from said first inverter on ~~the~~ an input terminal under ~~the~~ control of clock pulses, and a second switch for sending ~~the~~ an output signal from said first clocked inverter to the input terminal of said first inverter under ~~the~~ control of said ~~switching~~ switch control signal;

said second latch has a circuit under ~~the~~ control of said clock pulses for performing signal collection and signal retention in complementary relation to said first latch, a second inverter for generating an output signal to the input of said logic circuit , and a third inverter for generating an output signal for test scan;

said signal selector has a second clocked inverter

under ~~the~~ control of said switch control signal for receiving ~~the~~ a test input signal on ~~the~~ an input terminal, a third switch for sending ~~the~~ an output signal from said second clocked inverter to ~~the~~ an input of said second switch under ~~the switching~~ control of said clock pulses, and a signal generator for generating said ~~switching~~ switch control signal;

wherein said signal generator turns off said second clocked inverter by said operation mode signal during the normal operation, passing said clock pulses to said first and second switches as said switch control signal, in order to perform the complementary operation of signal collection and signal retention in response to the input signal by the first and second latches; and

wherein said signal generator turns off said first switch and turns on said second switch during the test mode in accordance with said operation mode signal, in order to perform the complementary operation of signal collection and signal retention by the first and second latches in response to the test input signal passing through said second clocked inverter ~~in the normal operation mode~~.

Claims 7-11 (Cancelled)